Self-Consistent FET Models for Amplifier Design and Device Diagnostics

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Abstract

A procedure has been developed for producing accurate and unique equivalent circuit models for carrier mounted GaAs FETs. The procedure incorporates zero drain-source bias S-parameter tests as well as Fukui-type, dc measurements. Data for 1 μm gate length, 600 μm periphery GaAs FETs are presented.

Introduction

Vaitus(1) has shown that the errors associated with measuring and de-embedding device scattering parameters (S-parameters) leads to significant error in the equivalent circuit element values for GaAs FETs. However, an accurate device modeling procedure would be an invaluable aid for device diagnostics and for amplifier development.

The purpose of our modeling effort was to develop a procedure for accurate determination of lumped-element equivalent circuit models for GaAs FETs mounted in various types of carriers. Four distinct problems have been addressed and solved in this study. They are:

1. Coaxial to microstrip transmission-line fixtures have been developed that provide accurate measurements from 2 to 20 GHz.
2. An accurate carrier model has been developed and verified, enabling the GaAs FET to be de-embedded.
3. An rf equivalent circuit for the GaAs FET has been developed that accurately models the device to 50 GHz.
4. A procedure for unequivocally determining the optimized values of the circuit elements has been found.

The de-embedding process was developed based upon wideband S-parameter measurements of device carriers without FET chips. Each mounted FET is studied separately to determine its parasitics. This is done by measurement of the S-parameters of the device with zero drain-source bias voltage, as Diamand and Laviron(2) have suggested. This test is an integral part of our method since the device model is much simpler in this state and the reactive elements of the mounting structure can be accurately resolved. Since the source, gate and drain resistances are not uniquely determined by the S-parameter data, they must be obtained by an independent measurement, such as the type described by Fukui(3). The final model for mounting parasitics is verified by checking that the parasitic element values do not change with gate-source biasing.

Dummy Package Measurements

S-parameter measurements were made on carriers without FET chips on the pedestals. The reference planes are the sides of the carrier as in the case of the device measurements. The S-parameter data for the ATC-S capacitors showed that the rf capacitance was very close to one half of the value measured in the low frequency bridge and well behaved up to 18 GHz.

Measurements were made for a 1.4 mm carrier with ATC-S capactiors and 76 μm gold ribbons from the capacitors to the .30 mm pedestal as in Fig. 1. Three equivalent circuit models were constructed. The first model contains all distributed elements (i.e. transmission lines). The second model used all lumped elements. The third was a mixture of lumped and distributed elements. The lumped element model provided the best agreement with the data and it is shown in the lower part of Fig. 1. The program SUPER-COMPACT(4) was used to optimize the element values for best agreement with the data. These data show that the pedestal inductance, L_3, is approximately 20 ph. The pedestal inductance

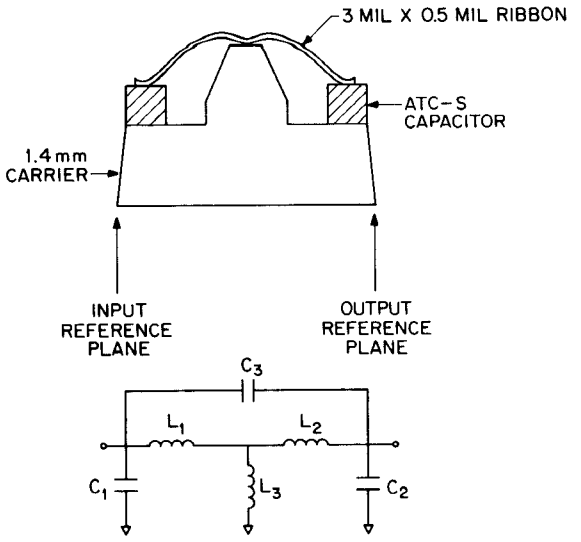

Figure 1. FET carrier model (lower) and cross-sectional view of carrier (upper).

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measured for three other carriers with .30 mm high pedestals is the same value within 5%. L_3 is present even for a zero-height pedestal. This result shows that pedestal inductance results from mutual inductance between the gate and drain leads.

The stability factor, K for an FET is

$$K = \frac{1 + |S_{11}\,S_{22} - S_{21}\,S_{12}|^2 - |S_{11}|^2 - |S_{22}|^2}{2\cdot|S_{12}|\cdot|S_{21}|}$$

Since we observed K values much larger than unity in the tests on the dummy carriers, there are losses associated with the carrier itself, probably resulting from radiation loss.

Zero Bias Measurements

The S-parameter measurements for a device with V_{ds} = 0 V permits more accurate evaluation of device parasitics because the device model is much simpler. Figure 2 shows the lumped element equivalent circuit for the case of zero biasing. Using S-parameter data for device 1824 - 20C for 4 to 18 GHz, all circuit element values were allowed to be optimized for minimum calculated error function in the program SUPER-COMPACT. For small differences in the error function, the optimum values of R_g, R_s and R_d were widely varying depending upon the method used for optimization and the starting values. It is interesting to note that the values of L_s, L_d, L_g, R and C did not vary more than ± 1% for these cases.

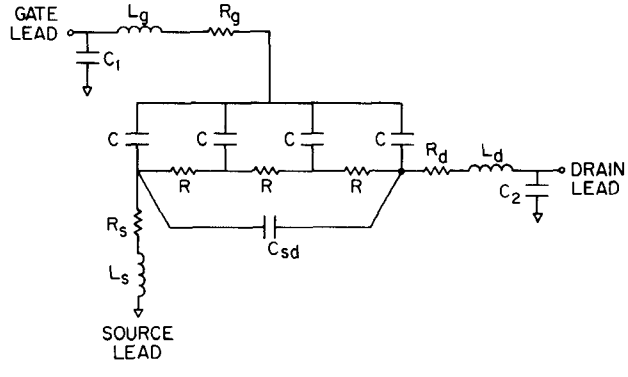

Figure 2. Equivalent circuit of carrier-mounted FET at zero drain-source bias voltage.

To resolve this accuracy problem, we decided to use resistance values determined from dc measurements of the type described by Fukui. Using these values, Table 1 shows the values of the other circuit elements for three values of V_{gs} for V_{ds} = 0. The values of R and C vary with gate bias as expected and the inductive circuit elements vary less than two percent.

Table 1. Optimized circuit element values for FET 1824-20C with V_{ds} = 0V for 4-18 GHz range with R_g = .549Ω, R_s = 1.048Ω, R_d = 1.367Ω, C_1 = .044pF, C_2 = .039 pF.

V_{gs} (V)	R (Ω)	C (pF)	C_{sd} (pF)	L_g (nH)	L_d (nH)	L_s (pH)
0.	.3354	.2289	.1730	.3115	.2514	10.71
-1.	.5143	.1814	.1726	.3134	.2507	10.73
-2.	.7593	.1620	.1725	.3158	.2516	10.48

FET Modeling at Full Bias Voltage

Subsequent S-parameter measurements at full operating bias can then be used to resolve the FET into an rf equivalent circuit of the type shown in Fig. 3. Using this procedure, the final FET model has only 8 unknown elements out of a possible 16. This circuit model has several important advantages over other configurations. The internal feedback capacitor C_i physically results from drain-to-channel feedback and causes the reverse transfer conductance (i.e. drain-to-gate) to have positive sign and square law frequency dependence. Such behavior is observed in our two-dimensional simulation(5) as well as in laboratory measurements. The current source is controlled by the total voltage across capacitor C_{sg} and resistor R_i rather than by the voltage across C_{sg} alone. This forces the time delay factor τ_t to account for all delay effects under the gate and permits the value of R_i to be based only upon input loss. By comparison with the two-dimensional models we have found this equivalent circuit model accurate to 50 GHz.

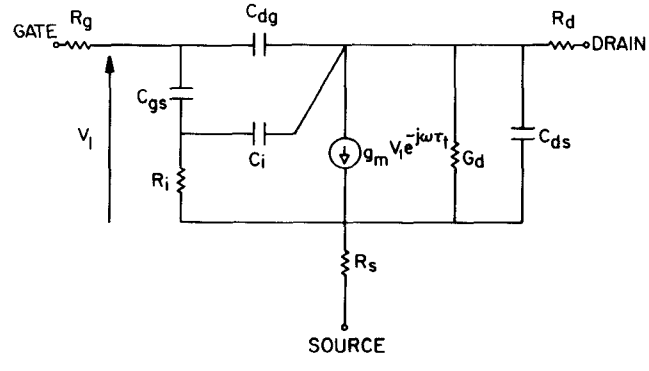

Figure 3. FET chip equivalent circuit at normal operating bias.

Values of the FET circuit elements are optimized for best agreement with the experimental data. It is interesting to compare the Y-parameters of the model with the Y-parameters found from the experimental data. The latter are obtained by de-embedding the device from the carrier.

Figure 4 shows the comparison of the model and data for Y_{11} for device 1824-20C. The accuracy becomes progressively worse as frequency is increased and the functional behavior with frequency is wrong above 18 GHz. The parameters Y_{21} and Y_{22} show similar behavior. This departure from the theoretically expected behavior means that only data up to 18 GHz should be used for fitting FET model parameters. Notice that the actual error between the data and final model is not large as the horizontal scale has been expanded for clarity in Fig. 4. The model was optimized for the frequency range 6-18 GHz. Optimization over a larger (or smaller) range does not change the functional form of the Y-parameters.

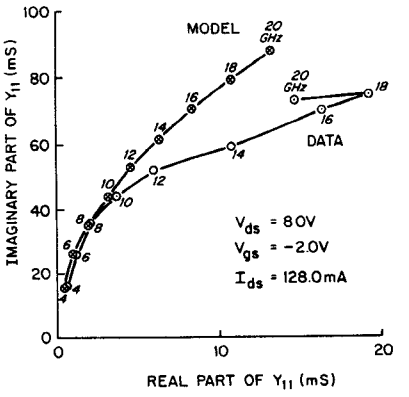

Figure 4. Admittance parameter Y_{11} as a function of frequency for the FET chip and for the de-embedded data.

Figure 5 shows the Smith chart valves of S_{11} and S_{22} computed using the FET model (including the carrier) and the measured data. Errors are small. An FET measured and modeled a second time (after disassembly from the test fixture) shows changes in the values of equivalent circuit elements of less than 10%.

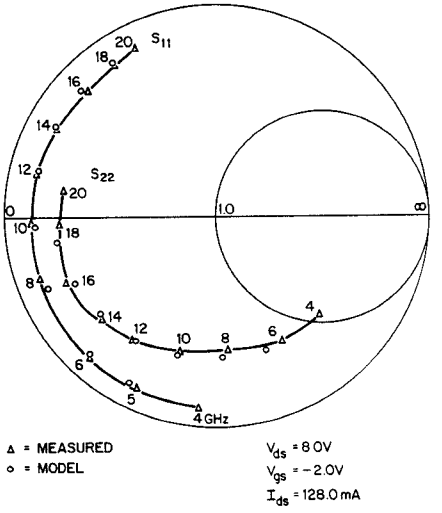

Figure 5. Smith chart display of measured data of model for the carrier mounted FET.

Convergence Considerations

SUPERCOMPACT is extremely useful for evaluating the values of the equivalent circuit for best agreement with the measured data. However, some element values are not uniquely determined and the resulting value will be a function of the search technique. We have found that:

1. Optimization should be done with the fewest possible unknown circuit elements.
2. Both random number and gradient search techniques should be used to assure that the results are convergent and independent of the starting values.
3. Some circuit element values may never converge for certain data sets.
4. Convergence of the important circuit elements occurs early in the search.

Evaluation of f_{MAX}

f_{MAX}, the frequency that maximum available gain (MAG) goes to zero dB is obtained by extrapolating the FET chip model (i.e. the de-embedded chip) in frequency using SUPER-COMPACT. However for this to be done accurately, it is necessary to achieve good agreement between the model and the data for the stability factor (as well as for S-parameters) over the range of measurement.

Figure 6 shows the stability factor obtained from the data for two separate measurements and from the model for the MESFET carrier with and without loss. The agreement is seen to be better for the lossy carrier. The loss added is 100 Ω in series with capacitors C_1 and C_2 shown in Fig. 1. The value of f_{max} obtained for the chip alone for either case is 34.0 GHz. If the data for the chip and carrier is used, an incorrect value of f_{max} of 24.0 GHz is obtained.

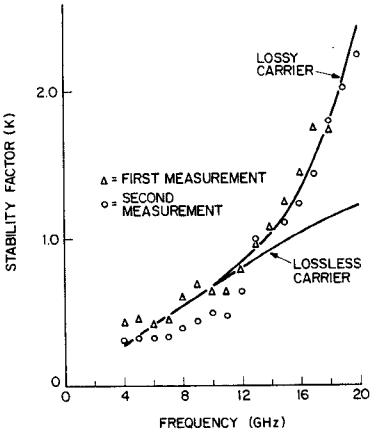

Figure 6. Stability factor as a function of frequency for the measured data and for the models.

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